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June 18, 2009

Examiner Brook Kebede
Group Art Unit 2894
U.S. Patent And Trademark Office
Alexandria, VA 22313-1450

RE: U.S. Patent Application Serial No. 10/604,912
Filed On August 8, 2003
Attorney Docket No. FIS920030026US1

Dear Examiner Kebede,

On May 8, 2009, the Board of Patent Appeals and Interferences noted that claim 9 (page 39, line 7) in the Appendix of Claims filed, on November 17, 2006, along with the Appellants' Appeal Brief should have read "forming spacers with a target spacer width adjacent to said gate stack, …" and not "forming spacers with a target spacer width adjacent to said gate, …". Therefore, the Board returned the application to the Examiner for correction of the Appendix of Claims.

Per your suggestion in our telephone call of June 15, 2009 and further per the Office Communication of June 18, 2009, the Applicants hereby submit the enclosed Appendix of

Claims to replace the original Appendix of Claims in the Appeal Brief. The enclosed Appendix of Claims properly reflects the language of claim 9, as entered.

Thank you for your assistance in this matter.

Respectfully submitted,

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IX. CLAIMS APPENDIX

1. A method of forming an integrated circuit transistor having a reduced gate height, said method comprising:

forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor;

patterning said laminated structure into at least one gate stack extending from said substrate;

forming spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width, a combined height of said gate conductor and said at least one sacrificial layer is predetermined;

doping regions of said substrate not protected by said spacers with an impurity to form source and drain regions adjacent said gate stack, wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor; and

removing said spacers and said sacrificial layer.

2. The method in claim 1, wherein said forming of said spacers adjacent said gate stack comprises forming said spacers adjacent said gate conductor and said at least one sacrificial oxide layer above said gate conductor.

3. (Cancelled).

4. The method in claim 1, wherein said forming of said spacers comprises forming said spacers so as to positions said source and drain regions further from said gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor.

5. The method in claim 1, wherein said sacrificial layer above said gate conductor is formed in a process comprising:

forming a sacrificial oxide layer above said gate conductor, and

forming additional sacrificial layers above said oxide layer.

6. The method in claim 5, wherein said sacrificial oxide layer protects said gate conductor.

7. The method in claim 1, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping process would implant said impurity through said gate conductor and said gate dielectric layer to said silicon

layer.

8. The method in claim 1, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process,

wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and said gate dielectric layer to said silicon layer.

9. A method of forming an integrated circuit transistor having a reduced gate height, said method comprising:

forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor;

patterning said laminated structure into at least one gate stack extending from said substrate;

forming spacers with a target spacer width adjacent to said gate stack, wherein

in order to achieve said target spacer width, a combined height of said gate conductor and said at least one sacrificial layer is predetermined;

epitaxially growing raised source and drain regions on said substrate adjacent said spacers;

after said epitaxially growing of said raised source and drain regions, implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions,

wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process and wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said raised source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor; and

removing said spacers and said sacrificial layer.

10. (Cancelled).

11. The method in claim 9, wherein said forming of said spacers comprises forming said spacers with said target spacer width so as to position~~s~~ said raised source and drain regions further from said gate conductor when compared to raised source and drain regions formed with spacers formed only to said height of said gate conductor.

12. The method in claim 9, wherein said sacrificial layer above said gate conductor is formed in a process comprising:

forming a sacrificial oxide layer above said gate conductor, and

forming additional sacrificial layers above said oxide layer,

wherein said sacrificial oxide layer protects said gate conductor.

13. The method in claim 9, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping process would implant said impurity through said gate conductor and said gate dielectric layer to said silicon layer.

14. The method in claim 9, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping

process,

wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and said gate dielectric layer to said silicon layer.

15. The method in claim 9, wherein by implanting said impurity after said epitaxially growing process, said impurity avoids being diffused as a result of said thermal budget of said epitaxially growing process.

16. A method of forming an integrated circuit transistor having a reduced gate height, said method comprising:

forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor;

patterning said laminated structure into at least one gate stack extending from said substrate;

forming spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width, a combined height of said gate conductor and said at least one sacrificial layer is predetermined;

epitaxially growing raised source and drain regions on said substrate adjacent said spacers, wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities;

after said epitaxially growing of said raised source and drain regions, implanting an impurity into said raised source and drain regions and into said

substrate below said raised source and drain regions,

wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process and wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said raised source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor; and

removing said spacers and said sacrificial layer.

17. The method in claim 16, wherein said forming of said spacers adjacent said gate stack comprises forming said spacers adjacent said gate conductor and said at least one sacrificial oxide layer above said gate conductor.

18. (Cancelled).

19. The method in claim 16, wherein said forming of said spacers comprises forming said spacers with said target spacer width so as to position~~s~~ said source and drain regions further from said gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor.

20. The method in claim 16, wherein said sacrificial layer above said gate conductor is formed in a process comprising:

forming a sacrificial oxide layer above said gate conductor, and

forming additional sacrificial layers above said oxide layer.

21. The method in claim 20, wherein said sacrificial oxide layer protects said gate conductor.

22. The method in claim 16, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping process would implant said impurity through said gate conductor and said gate dielectric layer to said silicon layer.

23. The method in claim 16, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process,

wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and said gate dielectric layer to said silicon layer.

24. A method of producing an integrated circuit transistor comprising:

forming a laminated stack deposition,

wherein said laminated stack deposition is formed in a process comprising:

forming a silicon layer over a substrate layer;

forming a gate oxide on said silicon layer;

forming a gate conductor on said gate oxide; and

forming of least one sacrificial material above said gate conductor,

patterning said gate oxide, gate conductor, and said sacrificial material into at least one gate stack;

forming temporary spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width, a combined height of said gate conductor and said at least one sacrificial layer is predetermined;

epitaxially growing raised source and drain regions above said substrate layer adjacent said temporary spacers, such that said temporary spacers separate said raised source and drain regions from said gate stack, wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities;

simultaneously implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions,

wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process and wherein said target spacer width is predetermined to ensure that said temporary spacers sufficiently separate said raised source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor;

growing an additional dielectric layer on said raised source and drain regions;

removing said temporary spacers without removing all of said sacrificial material;

performing a halo implant in said raised source and drain regions and in exposed regions of said silicon layer;

forming a permanent spacer adjacent said gate stack, wherein said permanent spacer is thinner than said temporary spacer;

performing a source and drain extensions implant in said raised source and drain regions and exposed regions of said silicon;

forming a final spacer filling said exposed regions of said silicon between said permanent spacer and said raised source and drain regions;

implanting additional impurities into said raised source and drain regions and exposed regions of said silicon;

annealing to activate all impurities;

etching back said additional dielectric layer on said raised source and drain regions; and

saliciding both said gate conductor and said raised source and drain regions.

25. (Cancelled).

26. The method in claim 24, wherein said removing of said sacrificial layer reduces the height of said gate conductor relative to the gate height associated with the spacing of the source and drain regions created by said spacers.

27. The method in claim 24, wherein said forming of said sacrificial material above said gate conductor further comprises forming a sacrificial oxide layer above said gate conductor, forming a sacrificial nitride layer above said oxide layer and forming a sacrificial hard insulator material above said nitride layer.

28. The method in claim 24, wherein said sacrificial oxide layer protects said gate conductor.